

II

Specifying Converters

Chapter 4

The applications for digital data-handling equipment and the products of the conversion-and-data-acquisition industry have spawned a multiplicity and diversity of companies, product lines, and products. We find it sobering (though not a little gratifying) to discover that, as a major manufacturer, with a reasonably complete line of modular products, we can deliver some 250 distinct D/A converter types, and that that line alone is growing by 75 types per year.

Thus the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence, to date, of standardized definitions of specifications among manufacturers.

To remedy this situation, and attempt to make the system designer's job of finding the "right" converter a little easier,* this chapter lists some of the elements of the decision and steps a user can take to help "home in" on a near-optimum selection. In this chapter are also summarized interpretations of the specifications consistent not only with the previous three chapters and with engineering practice at Analog Devices, but also — it is to be hoped — with interpretations that may become accepted as standard within the industry.

*It's possible that some of the points raised here, if previously unanticipated by the reader, may actually make the initial selection more involved, with the benefit that problems will be fewer at a later (and more expensive) stage.

A capsule selection guide is provided for the convenience of the engineer who may seek initial orientation to the various categories of devices available, in general, and to those available off-the-shelf from Analog Devices in particular. It is based on the 1972 Analog Devices catalog, which leads to the natural suggestion that the latest catalog available be consulted for specific choices. The reader is invited to request a copy from Analog Devices, either directly or via our nearest sales office.

Finally, a brief example of a data-acquisition design process, based on the suggestions in this chapter, is given.

TWO BASIC FACTORS

The two key factors in choosing the right device are:

Completely define the design objectives. Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interfaces, environmental conditions and space factors, anticipated budgetary limitations that may force performance compromises or a different system approach.

Understand what the specs mean. It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed (in 1972) that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. Two examples that give an insight into how differences arise are included and discussed at length in the Specifications section: *linearity* and *temperature coefficient*.

DEFINING THE OBJECTIVES – APPLICATION CHECKLISTS

General Considerations

- A. Accurate description of input and output
 - 1. Analog signal range; source or load impedance
 - 2. Digital code needed: Binary, 2's complement, BCD, etc.
 - 3. Logic-level compatibility: TTL, CMOS, etc., logic polarity
(Unless otherwise noted, logic levels mentioned in Analog Devices publications are standard TTL, positive true)
- B. Data throughput rate
- C. Control interface details
- D. What does the system error budget allow for each block?
- E. What are the environmental conditions: temperature range, supply voltage, re-calibration interval, etc., over which the converter should operate to the desired accuracy?
- F. Are there any special environmental conditions that must be coped with? High-power RF, high humidity, shock and vibration, and cramped space are a few.

In addition to the above general considerations, there are specific items to consider when choosing each block in a system.

Considerations for D/A Converters

- A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted? To what degree of accuracy, linearity, etc.?
- B. What logic levels and codes can be provided to the DAC? (The most popular logic system is TTL, and the most-frequently used codes are binary, 2's complement, offset binary (2's complement with a complemented MSB), as outputs of systems, and BCD, usually derived from digital voltmeters or thumbwheel switches.)
- C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier.

Voltage-output DAC's are the more convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μs and sub- μs settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., via CRT deflection amplifiers).

D. What kind of reference is needed, fixed (internal or external) or variable (multiplying DAC)? How many quadrants are needed, and how arranged, for multiplying DAC's (1-quadrant, 4-quadrant, 2-quadrant digital, 2-quadrant analog)?

E. What are the speed requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed (i.e., deglitched) within the DAC? What is the analog signal feedthrough requirement for multiplying DAC's at low frequencies? At high frequency?

F. Over how wide a temperature range (at the module, including its internal temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment? What deterioration of specifications is permitted (gain vs. linearity, etc.)

G. How stable are the terminal voltages of the power supplies that will power the DAC? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits?

Though no list can be complete, the above items will be the minimum considerations in any more-complete tabulation.

Considerations for A/D Converters

The process of selecting an A/D converter is similar to that involved in the selection of D/A converters. Some of the following considerations are analogous to those for D/A's, and others are unique to A/D's.

- A. What is the analog input range, and to what resolution must the signal be measured?
- B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?
- C. To what extent must the various sources of error be minimized as ambient temperature changes? Are missed codes tolerable under any conditions?
- D. How much time is allowed for each complete conversion?
- E. Is the reference to be fixed, adjustable, or variable (ratiometric measurement)?
- F. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system?
- G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Which conversion circuit philosophies are acceptable for, — or indicated by — the application? (e.g., successive-approximation, dual-slope integration, counter-&-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1MHz. Counter-comparator types provide lowest cost but may be both slow and noise-susceptible; they are useful for peak followers and sample-holds that employ digital storage.)

Considerations for Analog Multiplexers and Sample-Holds

When a sampled-data system is to be assembled, in which one A/D Converter is time-shared among many input channels by the use of a multiplexer and sample-hold, their contribution to system performance errors must be taken into account. These accessory devices are discussed in some detail in Part 3, but they are also discussed briefly in this chapter because of their relevance to the converter selection process.

Multiplexers

- A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?

- B. What kind of hierarchy is used, if a great many channels are involved? What is the addressing scheme?
- C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?
- D. How much ac crosstalk error between channels is allowable? At what frequencies?
- E. What error is produced by the leakage current flowing through the source resistance?
- F. What will be the multiplexer “transfer” error, produced by the voltage divider formed by the *on* resistance of the multiplexer and the input resistance of the sample-hold. Is the multiplexer active or passive (i.e., does it have an output amplifier?)
- G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test purposes?
- H. Is there danger of damage to active signal sources when the power is turned off? (MOSFET multiplexers are inherently “safe,” since the switches open when power is removed. JFET multiplexer switches can conduct when power is removed, making it possible to interconnect, and therefore damage active signal sources.

Sample-Holds

- A. What is the input signal range?
- B. Considering the slewing rate of the signal and the multiplexer’s channel-switching rate, what is the sample-hold’s allowable acquisition time to within the desired error band?
- C. What accuracy is needed (gain, linearity, and offset errors)?
- D. What aperture delay and jitter are allowable, going into *hold*? (The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, $1\text{V}/\mu\text{s}$ produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance, but jitter modulates the sampling rate.

- E. How much droop is allowable in *hold*?
- F. What are the effects of time, temperature, and power supply variation?
- G. What offset error is caused by the flow of the sample-hold's input bias current through the series resistance of the multiplex switch and the signal source?

DEFINING THE SPECIFICATIONS

Figures 1 and 2 depict the specifications of typical D/A and A/D converters. Though the specs probably mean "what you think they mean," it is important that their meaning and implications be spelled out. The following list, in alphabetical order, should prove helpful.

Absolute Accuracy. When a converter's full-scale point is adjusted, it will be set with respect to a reference voltage which, in turn can be traced to a recognized voltage standard. The *absolute accuracy* error of the converter is the tolerance of the full-scale set point referred to the *absolute* voltage standard.

Acquisition Time. The acquisition time of a sample-hold circuit is the time it takes to acquire the input signal to within the stated accuracy. When conservatively specified, as in Analog Devices' specifications, it includes the *settling time* of the output amplifier. Since it is possible, in some cases, for a signal to be fully acquired (and the circuit switched into *hold*) before the output has settled, one should be sure of what a manufacturer means by this term, since the output of the sample-hold is not meaningful until it has settled. (See the chapter on Sample-Holds.)

Common-Mode Range. Common-mode rejection usually varies with the magnitude of the range through which the input signal can swing, determined by the sum of the common-mode and the differential voltage. *Common-mode range* is that range of *total* input voltage over which specified common-mode rejection is maintained. For example, if the common-mode signal is $\pm 5\text{V}$ and the differential signal is $\pm 5\text{V}$, the common-mode range is $\pm 10\text{V}$.

Common-Mode Rejection. The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. It is usually expressed either as a ratio ($\text{CMRR} = 10^6$) or as $20 \log_{10}$

of the ratio ($CMR = 120dB$). A $CMRR$ of 10^6 means that a $10V$ common-mode voltage is processed by the device as though it were an additive differential input signal of $10\mu V$ magnitude.

Common-Mode Voltage. A voltage that appears in common at both input terminals of a device, with respect to its output reference (usually "ground"). For inputs V_1 and V_2 , with respect to ground, $CMV = \frac{1}{2}(V_1 + V_2)$. **Common-mode error** is any error at the output due to the common-mode input voltage.

DAC-QM AND DAC-QS		Digital-to-Analog Converters
SPECIFICATIONS (Typical @ +25°C unless otherwise noted)		
MODEL	DAC-QM	DAC-QS
RESOLUTION	- 8QM 8-bits -10QM 10-bits -12QM 12-bits	- 8QS 8-bits -10QS 10-bits -12QS 12-bits
DIGITAL INPUTS	"0" $E < +0.8V @ -3.2mA$ * "1" $+2 < E < +6V @ +80\mu A$ * TTL Compatible	*
STROBE	Data transfers from inputs to register on "0" to "1" change. Width at least 50ns, "0-1" transition at least 100ns after data change	No Strobe
INPUT CODES	Binary, 2's Compl., BCD, and their Complements	Complementary Binary only
OUTPUT RANGES (User programs with jumpers)	0 to +5V @ 10mA 0 to +10V @ 10mA $\pm 2.5V, \pm 5V, \pm 10V @ 10mA$	* * *
OUTPUT IMPEDANCE	0.02Ω	*
CONVERSION SPEED	$5\mu s$ to 0.01%	*
Slewing Rate	$20V/\mu s$	*
LINEARITY	$\pm \frac{1}{2}LSB$	*
ACCURACY ABSOLUTE	$\pm \frac{1}{2}LSB$	*
TEMP. COEFFICIENT		
Gain	$\pm 7ppm/^{\circ}C$ max	*
Zero	$\pm 15\mu V/^{\circ}C$ max	*
TEMP. RANGE		
Standard	$0^{\circ}C$ to $+70^{\circ}C$	*
Optional	$-55^{\circ}C$ to $+125^{\circ}C^I$	*
POWER REQUIRED	+15VDC @ +25mA -15VDC @ -30mA +5VDC @ +150mA	* * +5VDC @ +35mA
POWER SUPPLY SENSITIVITY	$0.002\%/%$ supply ΔE ($\pm 15VDC$ supplies only)	*
ADJUSTMENTS (User Provides)		
Gain Adj.	100Ω rheostat	$20k\Omega$ pot
Zero Adj.	$20k\Omega$ pot	*

Figure 1. Typical D/A Converter Specifications

ADC-QU ANALOG-TO-DIGITAL CONVERTERS SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL	ADC-QU
RESOLUTION	
ADC-8QU	8-bits
10QU	10-bits
12QU	12-bits
ACCURACY	
Relative	±½LSB
Quantization	±½LSB
Monotonicity	Monotonic from 0°C to +70°C
DIFFERENTIAL LINEARITY	<±½LSB
DIFFERENTIAL LINEARITY TC	±3ppm/°C, max (ADC-12QU)
TEMPERATURE COEFFICIENT	
Gain	±5ppm/°C of Range
Zero	±50µV/°C
Long Term Stability of Linearity	±½LSB typ
CONVERSION TIME	
ADC-8QU	6.4µs max (from trailing edge of convert
10QU	8µs max command to "1-0" change of
12QU	15µs max status signal)
INPUT VOLTAGE RANGES	±5V, ±10V, 0 to +10V, 0 to +5V, ±2.5V
INPUT IMPEDANCE	
Buffer	100 Megohms, min
Direct	
0 to +10V, or ±5V	5kΩ
0 to +5V, or ±2.5V	2.5kΩ
±10V	10kΩ
INPUT TRIGGER	Positive pulse, 100ns wide, min
(Convert Command)	Leading edge ("0" to "1") resets previous data
(see Figure 1)	Trailing edge ("1" to "0") initiates conversion
	TTL/DTL Compatible, 1 TTL/DTL Load
OUTPUT SIGNALS	Parallel, TTL/DTL Compatible; 4 TTL/DTL
(see Figure 1)	Loads/Bit
	Serial, RZ, TTL/DTL Compatible, 1 TTL/DTL Load
OUTPUT CODES	
Unipolar	Binary, BCD (Positive True)
Bipolar	Offset-Binary, 2's Complement (Positive True)
OUTPUT LEVELS	
"0"	<+0.4V
"1"	>+2.4V TTL/DTL Compatible
STATUS (see Figure 1)	"1" during conversion, 10 TTL/DTL Loads
STATUS COMPLEMENT	"0" during conversion, 4 TTL/DTL Loads
POWER SUPPLY REQUIREMENTS	+15V ±3% @ +25mA
(Separate Analog & Digital Grounds)	-15V ±3% @ -50mA Analog
	+5V ±5% @ 300mA Digital
POWER SUPPLY SENSITIVITY	±0.002%/°ΔV _S (±15V only)
TEMPERATURE RANGE	
Operating	0°C to +70°C*
Storage	-55°C to +125°C
ADJUSTMENTS	
(External Potentiometers Required)	
Zero:	100k pot across ±15 with 3 Meg in series w/slider to pin 20
Gain:	100k pot across ±15 with 30k in series w/slider to pin 1
DIMENSIONS	2" x 4" x 0.4" Module, Nominal

*Extended operating temperature versions available on special order.

Figure 2. Typical A/D Converter Specifications

Conversion Time. The time required for a complete measurement by an analog-to-digital converter. In successive-approximation converters, it ranges typically from $0.8\mu\text{s}$ (ADC-8F) to $400\mu\text{s}$ (ADC-16Q). Popular 12-bit general-purpose A/D converters, such as the ADC-12QM, have conversion time of about $25\mu\text{s}$.

Crosstalk. Leakage of signals between circuits or channels of a multi-channel system or device, such as a multiplexer. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent.

Degitcher (See *Glitch*). A device that removes or reduces the effects of time-skew pulses in D/A conversion. It normally consists of a sample-hold circuit, which holds the DAC output constant until the switches reach equilibrium. Since the phenomena involved can be extremely fast, the *degitcher* is usually a portion of the circuit, rather than a specific general-purpose modular device.

Differential Nonlinearity. In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 011. .11 to 100. . .00, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic*, or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of $\pm\frac{1}{2}\text{LSB}$ at 25°C ensures that monotonic behavior will exist over a tangible range of temperature, or each step is $(1 + \frac{1}{2})\text{LSB}$.

Differential-Nonlinearity Temperature Coefficient. Since bit weightings vary to some degree with temperature, a converter having acceptable differential nonlinearity at 25°C may have $>1\text{LSB}$ error at some other temperature. The temperature coefficient describes the maximum variation of differential linearity error with temperature over the specified range. Often, instead of a temperature coefficient, this specification may appear as a range of temperature for which behavior is monotonic.

Droop Rate. When a sample-hold circuit using a capacitor for storage is in *hold*, it will not hold the information forever. Droop rate is the rate at which the output voltage changes, and hence gives up information. As a rule, when using a SHA (sample-hold amplifier) ahead of an ADC, the SHA should not droop more than 0.1 LSB during the conversion time of the ADC.

Dual-Slope Converter. An integrating A/D converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a length of time determined by a counter. Then a reference input is switched to the integrator, which integrates “down” from the level determined by the unknown until a “zero” level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. The same counter and clock are used for this measurement, and thus the output is immune to long-term variations of the integrator’s characteristic time and the clock frequency. The counter provides the digital readout.

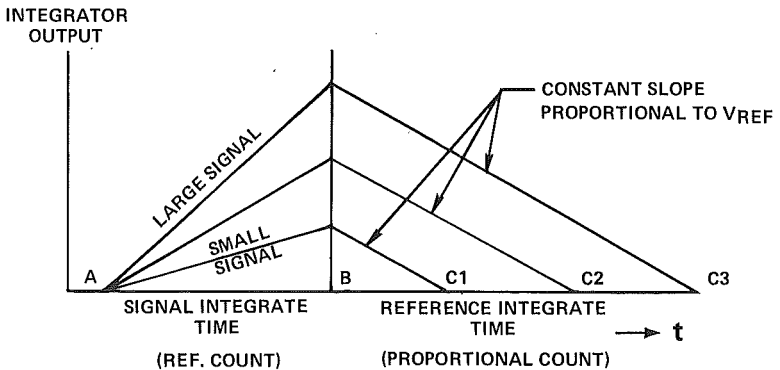


Figure 3. Voltage-Time Relationships in Dual-Slope Conversion

Feedthrough. A term referring to that characteristic of a circuit or device manifested by undesirable signal leakage around switches or other devices that are supposed to be turned off or provide isolation. Both digital and analog signals can cause analog feedthrough errors.

Four-Quadrant. In a *four-quadrant* multiplying DAC, if both the reference signal and the number represented by the input may be bipolar, the output can be either positive or negative, obeying the rules of multiplication as to algebraic sign in all four quadrants.

“Gain” Adjustment. The “gain” of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted either by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

“Glitch” If one applies the output of a counter to the input of a DAC to develop a “staircase” voltage, the number of bits involved in a code change establish “major” and “minor” transitions. The most major transition is at $\frac{1}{2}$ -scale, when the D/A switches all bits, i.e. from 011...111 to 1000...00. If the switches are faster to switch *off* than *on*, this means that, for a short time, the DAC will have zero output, and then return to the required 1LSB above the previous reading. This large transient spike is commonly known as a “glitch.” The better-matched the switching times, and the faster the switches, the smaller will be the energy contained in the glitch. (See also *Deglitcher*)

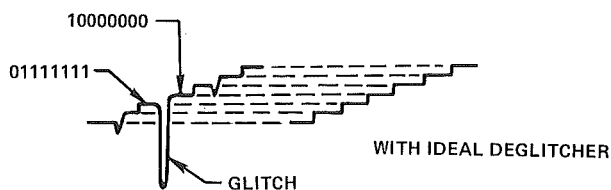


Figure 4. Glitch at a Major Carry

Least-Significant Bit (LSB). In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the *least-significant bit* is that digit (or “bit”) that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$), the rightmost “1” is the LSB. The weight of 1LSB, in relation to full scale, is the *resolution* implied by the digital number.

Linearity. The conventional definition for nonlinearity of a device is the deviation from a "best straight line." This means that, to determine whether a device meets the stated linearity specification, the "shape" of the nonlinearity and the magnitude have to be known so that the end points (e.g., the zero and full scale points for a unipolar converter) can be offset by a "best" amount to minimize linearity error. Since this definition is totally impractical for *users* of converters, Analog Devices defines nonlinearity as follows: the nonlinearity of a converter is the deviation from a straight line drawn between the end points, as calibrated by a normal adjustment procedure. As shown in Figure 5, this definition is more conservative than the "best straight line" since, if all errors are of the same polarity, they may only be half as great.

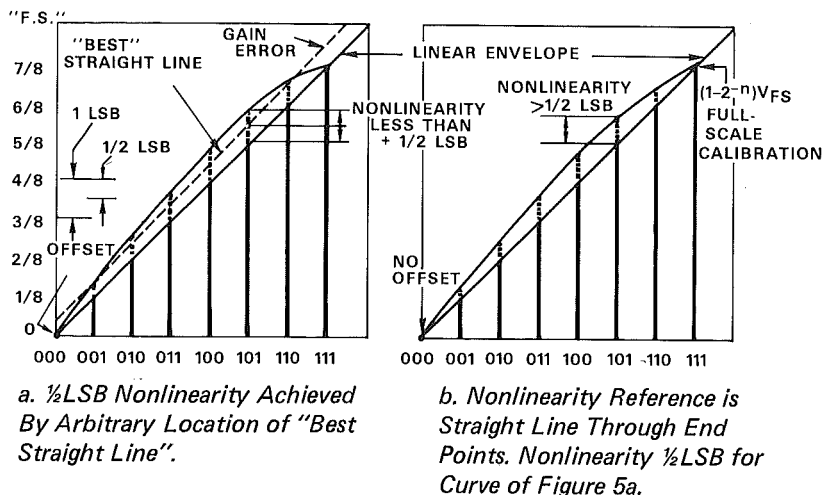


Figure 5. Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

The user of the converter now needs only to set the two end points to measure the nonlinearity. The normal limit that is used for a good converter is $\pm 1/2$ LSB, including the *differential nonlinearity*. This means that the sum of the positive errors or the sum of the negative errors of the individual bits must not exceed $1/2$ LSB,

which means further that the errors of the bits themselves must be considerably less than $\frac{1}{2}\text{LSB}$. For the higher-resolution converters (14 and 16 bits) from Analog Devices, the nonlinearity of *each and every code* is computed and plotted, to check performance before shipment. Linearity determines *relative accuracy* of converters. Once the converter has been adjusted and calibrated, deviations from linearity become absolute errors. While differential-linearity errors are cyclic, other linearity errors, such as might be caused by amplifier nonlinearity, tend to follow the usual nonlinearity patterns of other analog devices.

Monotonicity. The output of a monotonic D/A or A/D converter, in response to a continuously-increasing input signal A/D or count D/A should not, at any point, decrease or skip one or more codes. Monotonic behavior requires that the *differential nonlinearity* be $< 1\text{LSB}$. Integrating converters tend to be inherently monotonic. The higher-speed types that use D/A converters can be easily trimmed to be monotonic over a narrow temperature range, but for high resolutions over wide temperature ranges, switches and resistors must track very closely. Until the recent introduction of monolithic quad switches and film resistor networks (e.g., the μDAC 's) such converters had not been commonly available at reasonable cost.

Most Significant Bit (MSB). In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the *most-significant bit* is that digit (or "bit") that carries the greatest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$), the leftmost "1" is the MSB, with a weight of $\frac{1}{2}$ nominal peak-to-peak full scale. In bipolar devices, the sign bit is the MSB. In A/D converters having overrange bits, the MSB is the most-significant "overrange" bit.

Multiplying DAC. A multiplying DAC differs from the conventional fixed-reference DAC in being designed to operate with reference signals that vary, often at high speeds. The output signal of such a DAC is proportional to the product of the reference voltage and the fractional equivalent of the digital input number. In addition to the usual DAC specifications, the multiplying DAC

is specified as to analog signal *feedthrough* at low and high frequencies, and number of quadrants (1, 2-digital, 2-analog, or 4).

Noise. In high-resolution DAC's, such as the DAC-16QM, noise can be an important consideration, since the resolution is not confidently assignable when the peak noise exceeds the LSB value over a reasonable bandwidth. For an ADC, noise, either in the input signal, the input circuitry, or the conversion device itself, effectively increases the size of the quantization band, and may thus impart statistical properties to the output numbers, which may then require additional processing for successful interpretation.

Noise: RMS vs. Peak-to-Peak. For all but integrating converters, peak noise must be considered carefully, especially where small numbers of readings and limited processing capacity are available. An rms noise specification over a given bandwidth allows peak-to-peak predictions for gaussian noise (peak-to-peak values greater than 7x rms will probably occur less than 0.1% of the time). However, both peak-to-peak and rms noise specs should be looked at, since large spikes could be present on the output of a chopper-stabilized amplifier, or could be coupled into the analog portion of the system. These spikes, if narrow, will contribute little to driving the rms noise out of spec, but could nevertheless be considerably greater than 7x rms. If a DAC having spike noise on its output were used in a display system, the noise would cause distortion of the pattern, and loss of useful resolution.

Offset. For the great majority of bipolar converters (e.g., $\pm 10\text{V}$ output range), to obtain negative outputs corresponding to negative numbers, a unipolar device is used, offset by $\frac{1}{2}$ the full-scale range (instead of generating a set of negative values independently). For best results, this offset voltage or current is usually derived from the same reference supply that determines the scale factor of the converter, to make the zero-output point (of a D/A converter) independent of the thermal drift of the reference. The reason is that the $\frac{1}{2}$ -scale offset completely cancels the weight of the MSB at zero, independently of the amplitude.

Power-Supply Sensitivity. The sensitivity of a converter to changes in the power supplies is normally expressed in terms of percent

change in analog value (D/A output, A/D input) for a 1% change in power supply, e.g., $0.05\%/ \Delta V_s$. As a rule, the fractional change in scale factor should be well below the equivalent of $\pm \frac{1}{2}\text{LSB}$ for a 3% change in power-supply voltage. There should be no adverse effects on linearity or offset. When power-supply voltage changes affect conversion accuracy excessively, the key culprit is often a marginal “constant-current-circuit” for the reference diode.

Quantizing Uncertainty (or “Error”). The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of $\pm \frac{1}{2}\text{LSB}$, associated with the *resolution*, in addition to the actual conversion errors. This uncertainty is a property of the *system* resolution.

Relative Accuracy. Relative accuracy error is the difference between the nominal and actual ratios to full scale of the analog value corresponding to a given digital input, independently of the full-scale calibration. This error is a function of the linearity of the converter, and is usually specified at less than $\pm \frac{1}{2}\text{LSB}$.

Resolution. Nominal Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n , as a percentage, in parts-per-million, or simply by “n bits.” *Useful resolution* (not usually specified explicitly) is the smallest uniquely-distinguishable bit for all conditions of required operation (time, temperature, etc.) For example, a “12-bit” converter may have a useful resolution, over its temperature range, of only 10 bits. Useful resolution of DAC’s and devices using them (including ADC’s) is limited by the *relative accuracy*, but resolution need not limit accuracy. For example, a 4-bit D/A converter used in a programmable power supply has 16 levels, but it could have a required accuracy within 0.01% (absolute and/or relative. Note that low-cost completely-monolithic 8-bit DAC’s would not necessarily have sufficient accuracy for such an application, although their resolution is more than adequate.

Settling Time. This is the time it takes for a DAC to settle for a full-scale code change, usually to within $\pm \frac{1}{2}\text{LSB}$. For some

applications, e.g., in staircase waveform generation, a more important specification is the settling time for a single LSB change (at the major carry).

Slew(ing) Rate. The maximum rate at which an output voltage can change, in response to a full-scale-output demand. It is usually imposed by the availability of only limited current to charge a capacitor, either internally, or at the output, or by the tailoring of frequency response for some purpose such as dynamic stability. The output slewing speed of a modern digital-to-voltage converter is usually limited by the slew rate of the amplifier used at its output. Slew rate magnitude is usually a guide (but by no means infallible) to settling time.

Stability. In a well-designed intelligently-applied converter, *dynamic stability* is never a serious question. The term *stability* usually connotes the insensitivity of a converter's characteristics to time, temperature, etc. All measurements of instability are difficult and time-consuming (especially in high-resolution devices), but instabilities vs. temperature are sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see *temperature coefficient*).

Successive Approximations. A method of comparing an unknown against a group of weighted references (usually binary), capable of high speed. The process of successive approximations in an A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights, such as: 1 gram, ½ gram, ¼ gram, etc.

Switching Time. In a D/A Converter, the switching time is the time taken for an analog switch to change distinguishably to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time.

Temperature Coefficient (See also *Differential-Nonlinearity Temperature Coefficient*). Temperature coefficients of gain and offset are defined in terms of the "average" deviation over a range of temperature variation, i.e. $(\epsilon_{T_1} - \epsilon_{T_2}) / (T_1 - T_2)$. For specified temperature ranges that extend from below room temperature to above room temperature, the device is zeroed and calibrated at

room temperature, and the temperature coefficient for the “high” range ($T_H - T_R$) and for the “low” range ($T_R - T_L$) are both compared with the specification; both must be better than specified.

a. Gain TC This is affected by the reference zener ($< 5\text{ppm}/^\circ\text{C}$ for a good diode) and the reference circuitry, including the reference amplifier and switches. The total gain (or scale factor) change is specified in $\text{ppm}/^\circ\text{C}$.

b. Zero TC (unipolar converters) The zero stability of a unipolar DAC is almost entirely governed by the output amplifier’s zero stability. Since output amplifiers are usually employed essentially as current-to-voltage converters, they operate at low values of closed-loop gain, and the zero TC is not greatly affected by the choice of programmable gain setting (i.e., 0-5V or 0-10V). Zero TC is usually expressed in $\mu\text{V}/^\circ\text{C}$. Zero TC in ADC’s is generally dependent only on the zero stability of the input buffer amplifier (if included) and the comparator, and is expressed in $\mu\text{V}/^\circ\text{C}$, referred to the input.

c. Zero TC (bipolar converters) Converters that use offset-binary coding are “zero” set at the all-bits-off point, and their scale factor is set at either all-bits-on, or (for more precise zero) at the MSB transition. However, the zero TC is measured at the MSB transition (analog zero). It is affected by the reference TC, the tracking of the offset reference, and the tracking of the bipolar-offset and gain-setting resistors. For such precision DAC types as DAC-12QM, which use the same reference for both the scale factor and the MSB offset, and monolithic resistor networks (with their excellent tracking), the zero-TC specification is the same for both the unipolar and bipolar connections.

Zero Setting. The zero level of a unipolar DAC is set to zero volts at the code corresponding to 0V. The LSB transition of an ADC is offset by $\frac{1}{2}$ LSB, so that all subsequent transitions ideally occur midway between the nominal code values. (See also *offset* and *zero TC*.)

SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of "successive approximations:" Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy.

If its performance seems far in excess of that needed (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember, though, that in a maturing industry, costs can be expected to decline. *It is often less costly, in the long run, to go for better performance (rather than lowest possible cost) in the initial stages of a design.* Also, efforts aimed at reducing the cost of any element of a system should bear in mind the relationship of its cost relative to that of the entire project.

TYPICAL CONVERTER CLASSIFICATIONS

Once the problem is defined, and the key specifications have been determined, one is still faced with the question of narrowing the choice to devices likely to "fill the bill", as rapidly as possible, so as to conserve the time needed for actual evaluation. The "Capsule Selection Table" is a useful tool for accomplishing this objective of making a provisional selection. Tables 1, 2, and 3 illustrate examples of DAC, ADC, and sample-hold selection guides, as listed in the 1972 Analog Devices catalog. They contain a listing of products likely to fill a large fraction of conversion needs as of Spring 1972.* Their use is self-explanatory.

*Readers of this book are invited to communicate with ADI or our representatives for more recent listings, or to receive additional product suggestions for a given application.

Product Classification	General Purpose		Fast Display	Resolution	Multi- plying	MIL Grade I.C.
	Low Cost	High Performance				
Model Series	DAC-QZ DAC-Z MDA-Z	DAC-QS DAC-QM DAC-Q	DAC-DF ¹ MDA-F ²	DAC-QG DAC-16QM MDA-11MF ³ DAC-M ⁴ MDA-QD ⁵	AD560	
Resolution Bits	8	• • •	• • •	• • •	• • •	• • •
	10	• • •	• • •	• • •	• • •	• • •
	12	• • •	• • •	• • •	• • •	• • •
	14	• • •	• • •	• • •	• • •	• • •
	16	• • •	• • •	• • •	• • •	• • •
Input Codes	BIN	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	BCD	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Compl.	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Other	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Input Register	Yes	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	No	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Opt	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Output Signal	Current	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Voltage	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Both	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Output Range	Fixed	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Selectable	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Settling Speed	<200ns	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	200ns - 5μs	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	>5μs	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Tempco Gain in ppm/°C	<10	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	10-25	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	25-50	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
Package	Module	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Card	• • • • •	• • • • •	• • • • •	• • • • •	• • • • •
	Style	C-1 C-1 C-1	C-1 C-3 C-8	C-8 C-3	C-8 C-3	C-7 I.C. ⁶
Replaces	MDA-H DAC-H MDA-U MDA-L	DAC-T	DAC-10D	DAC-R		
Details on Page	74	76	78	80	82	84

¹ 200ns settling to 0.05% LSB changes.

² Settles to 0.05% in 40ns.

³ One or two quadrant, for use with very fast ramp reference; has 11-bit resolution.

⁴ Four quadrant, low frequency.

⁵ Very small hermetic package.

⁶ Ceramic DIL, 16 pins.

From Analog Devices, Inc.,
Product Guide, 1972

Table 1. Capsule Selection Table: Digital-to-Analog Converters

Product Classification		Low Cost General Purpose			High Performance General Purpose			Fast	High Resolution	Low Power	
Model Series		ADC-Z	ADC-H	ADC-S	ADC-QU	ADC-QM	ADC-Q	ADC-F	ADC-16Q ADC-I	ADC-QL	
Resolution Bits	8		•	•	•	•	•	•			
	10	•	•		•	•	•	•			
	12				•	•	•			•	
	16								•		
Convert Time Highest Resolution Version	17										
	Note								2	3	
	<1μs							•			
	1-10μs										
	10-50μs	•	•		•	•	•				
Range	>50μs			• ¹					•	•	
	Fixed		•				•	•		•	
Output	Selectable	•		•	•	•			•	•	
	Serial								•		
	Parallel			•		•		•	•		
Codes Available	Both	•	•		•		•		•	•	
	BIN	•	•	•	•	•	•	•	•	•	
	BCD		•	•	•	•	•		•		
Tempco ppm/°C Highest Resolution Version	Other		•		•	•	•		•		
	<10				•	•	•		•	•	
	10-25									•	
	25-50	•	•					•			
Package	>50			•							
	Card					•		•	•	•	
	Module	•	•	•	•	•			•		
Style		C-3	C-3	C-2	C-3	C-3	C-8	C-6	C-8	C-5	C-8
Replaces		ADC-T, ADC-U									
Details on Page		86			88			94	90	92	

¹ Convert time 1ms FS.

² 400 μ s without buffer.

³ Dual slope integrator; 40ms.

From Analog Devices, Inc., Product Guide, 1972

Table 2. Capsule Selection Table: Analog-to-Digital Converters

APPLICATIONS	General Purpose	Fast	Low Droop Slow Settle	Low Droop Fast Settle	Low Cost
	SHA-1A	SHA-2A	SHA-3	SHA-4	SHA-5
Data Acquisition					
1-15 μ s/sample	•	•			
15-80 μ s/sample					
80-250 μ s/sample					•
>250 μ s/sample			•	•	
Suggested for Use With These A/D Converters					
ADC-F		•			
ADC-H	•				•
ADC-I			•	•	
ADC-Q	•				
ADC-QM	•				
ADC-QU	•	•			
ADC-S				•	•
ADC-Z	•				•
Data Distribution*					
Fast (20ms between updates)	•				
Slow (100ms between updates)			•	•	•
Suitable for Systems With Following Limit of Linearity Errors:					
0.05%		•			•
0.01%	•		•	•	
Details on Page	96	96	96	96	96

*For Data Distribution, use any DAC of appropriate resolution. Those with internal registers (DAC-QM) may be most convenient.
From Analog Devices, Inc., Product Guide, 1972

Table 3. Capsule Selection Table: Sample and Hold Amplifiers

AN EXAMPLE OF THE SELECTION AND VERIFICATION PROCESS*

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers $\pm 10V$ full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

*For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the less-salient sources of error have been intentionally omitted. If there are any that you're concerned about for your application but don't see here, we invite you to communicate with our Applications Engineers.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is $+25^{\circ}\text{C}$ to $+55^{\circ}\text{C}$. Sufficient power at both $\pm 15\text{V}$ and $+5\text{V}$ is available, but the regulation of the $\pm 15\text{V}$ supply is 150mV .

The objective: specify a set of conversion components having appropriate accuracy and speed.

FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with compatible multiplexer and sample-hold.

Reviewing the available A-D converters, we find the ADC-12Q and ADC-12QM to be possible choices. If the entire system is to be built on a single card, the ADC-12QM, a 2" x 4" x 0.4" encapsulated module would be a convenient choice.

The ADC-12QM completes a conversion in $25\mu\text{s}$. For sample-hold, the compatible SHA-1A is chosen, adding $5\mu\text{s}$ of settling time. Thus, the combination appears to be amply capable of meeting the $50\mu\text{s}/\text{channel}$ scanning requirement. Since the multiplexer will scan sequentially, its settling time is inconsequential. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least $25\mu\text{s}$ to settle before a measurement is called for. For convenience, one may use the MPX-8A; the small 2" x 2" x 0.4" module fits into the packaging concept, and the built-in complete binary-address decoding makes it easy to work with.

ERROR ANALYSIS

It's clear that the MPX-8A, the SHA-1A, and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to

determine if the worst-case situation is within the allowable 0.1% system error.

Multiplexer

The switches of the MPX-8A, being MOSFET's, with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.

Leakage current @ 25°C 10nA

Source impedance 10Ω

Error voltage = $10 \times 10 \times 10^{-9} = 10^{-7} \text{ V}$ (negligible)

2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the SHA-1A:

ON resistance 1000Ω maximum

SHA-1A R_{in} $10^{12}\Omega$

Divider ratio attenuation error: 10^{-9} (negligible)

Sample-Hold

1. Nonlinearity is 2mV over the 20V range, or 0.01%
2. Gain error of 0.05% maximum (and other similarly small initial gain errors in the system) may be compensated for overall when calibrating the system by setting the scale constant of the ADC. It is not considered as part of the error budget.
3. Input bias current of 10na (max) causes an offset error voltage in the source resistance.

Source resistance = 10Ω (source) + 1kΩ(MPX switch)

Offset error = $10^3 \times 10^{-8} = 10\mu\text{V}$ (negligible)

4. Offset vs. temperature = $25\mu\text{V}/^\circ\text{C}$

Since the temperature inside the housing may change by as much as 30°C, the total change over the range will be

$$25 \times 30 = 750\mu\text{V}, \text{ or } 75 \text{ ppm of } \pm 10\text{V}$$

An offset adjustment is provided for initial trimming.

5. Offset vs power supply = $100\mu\text{V}/\% \Delta V_s$

Since the supply may vary by 150mV, or 1% of 15V, the error contribution is 100 μ V, or 0.001% of full scale.

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate-and settling-time allowances. However, the components selected for this example have more than adequate settling time, even for 0.01% operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Converter

1. Specified linearity error (relative accuracy) $\frac{1}{2}$ LSB, or 0.0125%.
2. Quantizing uncertainty: $\frac{1}{2}$ LSB, or 0.0125%. This is a resolution limitation, not normally considered in the error budget.
3. Temperature errors
 - a. Gain temperature coefficient: 5ppm/ $^{\circ}$ C for 30 $^{\circ}$ C
 $5 \times 30 = 150$ ppm, or 0.015%
 - b. Zero temperature coefficient: 5ppm/ $^{\circ}$ C for 30 $^{\circ}$ C
 $5 \times 30 = 150$ ppm, or 0.015%
4. Power supply sensitivity error: 0.002%/ % ΔV_s ,
 For a 1% shift, the error is 20ppm
5. Differential nonlinearity temperature coefficient, 3ppm/ $^{\circ}$ C.
 For 30 $^{\circ}$ C temperature change, error is 90ppm, less than $\frac{1}{2}$ LSB.
 Therefore, 12-bit monotonicity can be maintained, with no missing codes.

CONCLUSION

In this example, the worst-case arithmetic sum of these errors is 0.07%, and the rms sum is 0.03%. Since these values are reasonably conservative for a system with specified error of 0.1%, the designer may either rest with these choices and go on to the more-difficult hardware, software, interface, and wiring problems, or — if absolute-minimum cost of conversion hardware is an important objective — seek to reduce cost by considering a more marginal design.

In this chapter, we have sought to help the designer in his process of choosing a converter by providing checklists of relevant questions in making a choice, definitions of specifications and related features, a capsule selection guide, and an example of selection and evaluation. We now go on to some considerations for what must be done to make the system work as expected.